METHODS FOR WAFER-LEVEL PACKAGING OF MICROELECTRONIC DEVICES AND MICROELECTRONIC DEVICES FORMED BY SUCH METHODS

ABSTRACT OF THE DISCLOSURE

Methods for packaging microelectronic devices, microelectronic workpieces having packaged dies, and microelectronic devices are disclosed herein. One aspect of the invention is directed toward a microelectronic workpiece comprising a substrate having a device side and a backside. In one embodiment, the microelectronic workpiece further includes a plurality of dies formed on the device side of the substrate, a dielectric layer over the dies, and a plurality of bond-pads on the dielectric layer. The dies have integrated circuitry and a plurality of bond-pads electrically coupled to the integrated circuitry. The ball-pads are arranged in ball-pad arrays over corresponding dies on the substrate. The microelectronic workpiece of this embodiment further includes a protective layer over the backside of the substrate. The protective layer is formed on the backside of the substrate from a material that is in a flowable state and is then cured to a non-flowable state.